



FPGA Module SPI Flash Write Issue:

FPGA PROG Pin Solution

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The entire family of DLP Design USB-to-FPGA modules (the DLP-FPGA, DLP-HS-FPGA and DLP-HS-FPGA2) uses a SPI flash device to configure the FPGA. This article addresses a problem that can occur which causes our BitLoadApp configuration utility to fail on a write to the SPI flash. To resolve this issue, we must first understand the FPGA configuration process.

The FPGA has internal configuration circuitry that is always present. When the module's power is first applied, or when the FPGA's PROG line transitions from low to high, the configuration circuitry reads data sequentially from the SPI flash. The FPGA must encounter a specific sequence of bytes in the serial data stream in order to initialize the configuration circuitry and program the FPGA. This is called a synchronization sequence.

If the SPI flash has been written with a *.bit file that is not a valid bit stream or the write gets corrupted, this synchronization sequence can be missing from the data in the SPI flash. If the sequence is missing, the configuration circuitry will continue to read through the entire SPI flash looking for it. Since this is a serial flash, the read will wrap around from the end of the SPI flash to its beginning looking for the synchronization sequence. In this way, the configuration circuitry can get stuck in a loop continuously cycling through the SPI flash looking for the synchronization sequence. When this happens, the BitLoadApp cannot successfully write to the SPI flash because at the same time that the BitLoadApp is trying to write to the SPI flash, the FPGA's configuration circuitry is trying to read from it.

Once in this condition, the FPGA configuration circuitry must be forced to stop reading from the SPI flash to allow the BitLoadApp to write to it. In order to do this, the FPGA's PROG pin must be pulled low, which disables the FPGA's configuration circuitry. To pull PROG low on any of the DLP Design FPGA modules, the user must short across the PROG jumper pins on the module. The PROG jumper location on the DLP Design FPGA modules is shown in the following image:



The user must hold the short across the PROG pins in place while using the BitLoadApp to write a valid configuration file into the SPI flash. When the write is complete, just remove the short, and the FPGA configuration will succeed. At this point, the BitLoadApp will work properly.