Command Processor For MPSSE and MCU Host Bus Emulation Modes

Overview

The FT2232C incorporates a command processor called the Multi-Protocol Synchronous Serial Engine (MPSSE). The purpose of the MPSSE command processor is to communicate with devices which use synchronous protocols (such as JTAG or SPI) in an efficient manner. The FT2232Cs MCU Host Bus Emulation mode also uses the MPSSE technology to make the chip emulate a standard 8048 / 8051 MCU host bus.

The MPSSE Command Processor unit is controlled using a SETUP command. Various commands are used to clock data out of, and into the chip, as well as controlling the other I/O lines. If disabled the MPSSE is held reset and will not have any effect on the rest of the chip. When enabled it will take its commands and data from the OUT data written to the OUT pipe in the chip. This is done by simply using the normal WRITE command, as if data were being writen to a Com port. Any data read will be passed back in the normal IN pipe. This is done using the normal READ command, as if data were being read from a Com port.

Data Bit Definition

Data Bit	Signal	FT2232C Pin	Type	Description
Bit0	TCK/SK	ADBUS0	Output	Clock Signal Output
Bit1	TDI/DO	ADBUS1	Output	Serial Data Out
Bit2	TDO/DI	ADBUS2	Input	Serial Data In
Bit3	TMS/CS	ADBUS3	Output	Select Signal Out
Bit4	GPIOL1	ADBUS4	Input / Output	General Purpose I/O
Bit5	GPIOL2	ADBUS5	Input / Output	General Purpose I/O
Bit6	GPIOL3	ADBUS6	Input / Output	General Purpose I/O
Bit7	GPIOL4	ADBUS7	Input / Output	General Purpose I/O
Bit8	GPIOH1	ACBUS0	Input / Output	General Purpose I/O
Bit9	GPIOH2	ACBUS1	Input / Output	General Purpose I/O
Bit10	GPIOH3	ACBUS3	Input / Output	General Purpose I/O
Bit11	GPIOH4	ACBUS4	Input / Output	General Purpose I/O

Clock Operation

The clock will do an XOR of the current state of the TCK/SK pin twice. This means that if the clock pin is set low, then the clock will go high then low to be 1 clock cycle. If the clock pin were set high, then the clock will go low then high to be 1 clock cycle.

Command Definitions

Bad Commands

If the device detects a bad command it will send back 2 bytes to the PC.

0xFA,
followed by the bad command byte.

If the data has got out of sequence then this can be used to determine what that the first pattern was, and that an error was detected. The error may have occurred before this, (for example sending the wrong amount of data after a write command) and will only trigger when bit 7 of the rogue command is high.

Data Shifting Commands Overview

The data shifting commands are made up of the following definitions :

Bit 0 : -ve TCK/SK on write
Bit 1 : bit mode = 1 else byte mode
Bit 2 : -ve TCK/SK on read
Bit 3 : LSB first = 1 else MSB first
Bit 4 : Do write TDI/DO
Bit 5 : Do read TDO/DI
Bit 6 : Do write TMS/CS
Bit 7 : 0

Write commands to TDI/DO take effect when bits 7 and 6 are ‘0’. Read TDO/DI will operate with TMS/CS output, or TDI/DO output, or on its own.

MSB First

1. Clock Data Bytes Out on +ve Clock Edge MSB First (no Read) (use if TCK/SK starts at '1')

0x10,
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

This will clock out bytes on TDI/DO from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte, and a length of 0xffff will do 65536 bytes. The data is sent MSB first. Bit 7 of the first byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the rising edge of the TCK/SK pin.

2. Clock Data Bytes Out on -ve Clock Edge MSB First (no Read) (use if TCK/SK starts at '0')

0x11,
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

This will clock out bytes on TDI/DO from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The data is sent MSB first. Bit 7 of the first byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the falling edge of the TCK/SK pin.

3. Clock Data Bits Out on +ve Clock Edge MSB First (no Read) (use if TCK/SK starts at '1')

0x12,
Length,
Byte1

This will clock out bits on TDI/DO from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data is sent MSB first. Bit 7 of the data byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the rising edge of the TCK/SK pin.

4. Clock Data Bits Out on -ve Clock Edge MSB First (no Read) (use if TCK/SK starts at '0')

0x13,
Length,
Byte1

This will clock out bits on TDI/DO from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data is sent MSB first. Bit 7 of the data byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the falling edge of the TCK/SK pin.

5. Clock Data Bytes In on +ve Clock Edge MSB First (no Write)

0x20,
LengthL,
LengthH

This will clock in bytes on TDO/DI from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The first bit in will be the MSB of the first byte and so on. The data will be sampled on the rising edge of the TCK/SK pin.

6. Clock Data Bytes In on -ve Clock Edge MSB First (no Write)

0x24,
LengthL,
LengthH

This will clock in bytes on TDO/DI from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The first bit in will be the MSB of the first byte and so on. The data will be sampled on the falling edge of the TCK/SK pin.

7. Clock Data Bits In on +ve Clock Edge MSB First (no Write) (TDO/DI sampled just prior to rising edge)

0x22,
Length,

This will clock in bits on TDO/DI from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data will be shifted up so that the first bit in may not be in bit 7 but from 6 downwards depending on the number of bits to shift (i.e. a length of 1 bit will have the data bit sampled in bit 0 of the byte sent back to the PC). The data will be sampled on the rising edge of the TCK/SK pin.

8. Clock Data Bits In on -ve Clock Edge MSB First (no Write) (TDO/DI sampled just prior to falling edge)

0x26,
Length,

This will clock in bits on TDO/DI from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit, and a length of 0x07 will do 8 bits. The data will be shifted up so that the first bit in may not be in bit 7 but from 6 downwards depending on the number of bits to shift (i.e. a length of 1 bit will have the data bit sampled in bit 0 of the byte sent back to the PC). The data will be sampled on the falling edge of the TCK/SK pin.

9. Clock Data Bytes In and Out MSB First

0x30, out on +ve edge, in on +ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

or

0x31, out on -ve edge, in on +ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

or

0x34, out on +ve edge, in on -ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

or

0x35, out on -ve edge, in on -ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

10. Clock Data Bits In and Out MSB First

0x32, Length Byte — out on +ve edge, in on +ve edge

or

0x33, Length Byte — out on -ve edge, in on +ve edge

or

0x36, Length Byte — out on +ve edge, in on -ve edge

or

0x37, Length Byte — out on -ve edge, in on -ve edge

LSB First

11. Clock Data Bytes Out on +ve Clock Edge LSB First (no Read) (use if TCK/SK starts at '1')

0x18,
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

This will clock out bytes on TDI/DO from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The data is sent LSB first. Bit 0 of the first byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the rising edge of the TCK/SK pin.

12. Clock Data Bytes Out on -ve Clock Edge LSB First (no Read) (use if TCK/SK starts at '0')

0x19,
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

This will clock out bytes on TDI/DO from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The data is sent LSB first. Bit 0 of the first byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the falling edge of the TCK/SK pin.

13. Clock Data Bits Out on +ve Clock Edge LSB First (no Read) (use if TCK/SK starts at '1')

0x1A,
Length,
Byte1

This will clock out bits on TDI/DO from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data is sent LSB first. Bit 0 of the data byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the rising edge of the TCK/SK pin.

14. Clock Data Bits Out on -ve Clock Edge LSB First (no Read) (use if TCK/SK starts at '0')

0x1B,
Length,
Byte1

This will clock out bits on TDI/DO from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data is sent LSB first. Bit 0 of the data byte is placed on TDI/DO then the TCK/SK pin is clocked. The data will change to the next bit on the falling edge of the TCK/SK pin.

15. Clock Data Bytes In on +ve Clock Edge LSB First (no Write)

0x28,
LengthL,
LengthH

This will clock in bytes on TDO/DI from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The first bit in will be the LSB of the first byte and so on. The data will be sampled on the rising edge of the TCK/SK pin.

16. Clock Data Bytes In on -ve Clock Edge LSB First (no Write)

0x2C,
LengthL,
LengthH

This will clock in bytes on TDO/DI from 1 to 65536 depending on the Length bytes. A length of 0x0000 will do 1 byte and a length of 0xffff will do 65536 bytes. The first bit in will be the LSB of the first byte and so on. The data will be sampled on the falling edge of the TCK/SK pin.

17. Clock Data Bits In on +ve Clock Edge LSB First (no Write) (TDO/DI sampled just prior to rising edge)

0x2A,
Length,

This will clock in bits on TDO/DI from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data will be shifted down so that the first bit in may not be in bit 0 but from 1 upwards depending on the number of bits to shift (i.e. a length of 1 bit will have the data bit sampled in bit 7 of the byte sent back to the PC). The data will be sampled on the rising edge of the TCK/SK pin.

18. Clock Data Bits In on -ve Clock Edge LSB First (no Write) (TDO/DI sampled just prior to falling edge)

0x2E,
Length,

This will clock in bits on TDO/DI from 1 to 8 depending on the Length byte. A length of 0x00 will do 1 bit and a length of 0x07 will do 8 bits. The data will be shifted down so that the first bit in may not be in bit 0 but from 1 upwards depending on the number of bits to shift (i.e. a length of 1 bit will have the data bit sampled in bit 7 of the byte sent back to the PC). The data will be sampled on the falling edge of the TCK/SK pin.

19. Clock Data Bytes In and Out LSB First

0x38, out on +ve edge, in on +ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

or

0x39, out on -ve edge, in on +ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

or

0x3C, out on +ve edge, in on -ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

or

0x3D, out on -ve edge, in on -ve edge
LengthL,
LengthH,
Byte1
..
Byte65536 (max)

20. Clock Data Bits In and Out LSB First

0x3A, Length Byte — out on +ve edge, in on +ve edge

or

0x3B, Length Byte — out on -ve edge, in on +ve edge

or

0x3E, Length Byte — out on +ve edge, in on -ve edge

or

0x3F, Length Byte — out on -ve edge, in on -ve edge

21. Clock Data to TMS/CS Pin (no Read)

0x4A or 0x4B
Length,
Byte1

This will send data bits 6 down to 0 to the TMS/CS pin using the LSB or MSB and -ve or +ve TCK/SK , depending on which of the lower bits have been set.

0x4A : TMS/CS with LSB first on +ve TCK/SK edge - use if TCK/SK is set to '1'
0x4B : TMS/CS with LSB first on -ve TCK/SK edge - use if TCK/SK is set to '0'

Bit 7 of the Byte1 is passed on to TDI/DO before the first TCK/SK of TMS/CS and is held static for the duration of TMS/CS clocking. No read operation will take place.

22. Clock Data to TMS/CS Pin with Read

0x6A or 0x6B or 0x6E or 0x6F
Length,
Byte1

This will send data bits 6 down to 0 to the TMS/CS pin using the LSB or MSB and -ve or +ve TCK/SK , depending on which of the lower bits have been set.

0x6A : TMS/CS with LSB first on +ve TCK/SK edge, read on +ve edge - use if TCK/SK is set to '1'
0x6B : TMS/CS with LSB first on -ve TCK/SK edge, read on +ve edge - use if TCK/SK is set to '0'
0x6E : TMS/CS with LSB first on +ve TCK/SK edge, read on -ve edge - use if TCK/SK is set to '1'
0x6F : TMS/CS with LSB first on -ve TCK/SK edge, read on -ve edge - use if TCK/SK is set to '0'

Bit 7 of the Byte1 is passed on to TDI/DO before the first TCK/SK of TMS/CS and is held static for the duration of TMS/CS clocking. The TDO/DI pin is sampled for the duration of TMS/CS and a byte containing the data is passed back at the end of TMS/CS clocking.

23. Set Data Bits Low Byte

0x80,
0xValue,
0xDirection

This will setup the direction of the first 8 lines and force a value on the bits that are set as output. A 1 in the Direction byte will make that bit an output.

24. Set Data Bits High Byte

0x82,
0xValue,
0xDirection

This will setup the direction of the high 4 lines and force a value on the bits that are set as output. A 1 in the Direction byte will make that bit an output.

25. Read Data Bits Low Byte

0x81,

This will read the current state of the first 8 pins and send back 1 byte.

26. Read Data Bits High Byte

0x83,

This will read the current state of the high 4 pins and send back 1 byte.

27. Connect TDI/DO to TDO/DI for Loopback

0x84,

This will connect the TDI/DO output to the TDO/DI input for loopback testing.

28. Disconnect TDI/DO to TDO/DI for Loopback

0x85,

This will disconnect the TDI/DO output from the TDO/DI input for loopback testing.

29. Set TCK/SK Divisor

0x86,
0xValueL,
0xValueH,

This will set the clock divisor.

The TCK/SK duty cycle is always 50%, except between commands where it will remain in its initial state. The initial state is set using the **23. Set Data Bits Low Byte** command. For example, to use it in JTAG mode you would issue :-

$80 Set Data Bits Low Byte
$08 TCK/SK, TDI/DO low, TMS/CS high
$0B TCK/SK, TDI/DO, TMS/CS output, TDO/DI and GPIOL1 -> 14 input

The clock will then start low. When the MPSSE is sent a command to clock bits (or bytes) it will make the clock go high and then back low again as 1 clock period. For TMS/CS commands a $4B command would be used for no read, and a $6B command for TMS/CS with read. For clocking data out on TDI/DO with no read of TDO/DI, a $19 command would be used for bytes, and $1B for bits. To read from TDO/DI with no data sent on TDI/DO a $28 command would be used for bytes, and $2A for bits. To scan in and out at the same time a $39 command would be used for bytes, and $3B for bits.

The TCK/SK frequency can be worked out using the following algorithm :

TCK/SK period = 12MHz / ((1 +[(0xValueH * 256) OR 0xValueL]) * 2)

For example:

Value	TCK/SK max
0x0000	6 MHz
0x0001	3 MHz
0x0002	2 MHz
0x0003	1.5 MHz
0x0004	1.2 MHz
.....	.....
0xFFFF	91.553 Hz

Instructions for MCU Host Bus Emulation Mode

MCU Host Bus Emulation mode makes the chip emulate a CPU with :

a) a multiplexed 8 bit address and data bus
b) an extended 8 bit address bus
c) CS# , ALE , WR# , RD# and OSC signals
d) 2 I/O lines that can be used as extra I/O or to wait for IRQs. These are defined as I/O0 and I/O1.

30. MCU Host Emulation Mode Read Short Address

0x90,
0xAddrLow

This will read 1 byte.

31. MCU Host Emulation Mode Read Extended Address

0x91,
0xAddrHigh
0xAddrLow

This will read 1 byte.

32. MCU Host Emulation Mode Write Short Address

0x92,
0xAddrLow,
0xData

This will write 1 byte.

33. MCU Host Emulation Mode Write Extended Address

0x93,
0xAddrHigh,
0xAddrLow,
0xData

This will write 1 byte.

Instructions for use in both MPSSE and MCU Host Emulation Modes

34. Send Immediate

0x87,

This will make the chip flush its buffer back to the PC.

35. Wait On I/O High

0x88,

This will cause the controller to wait until GPIOH1 (MPSSE) or I/O1 (MCU Host Bus Emulation) is high. Once it is detected as high, it will move on to process the next instruction. The only way out of this will be to disable the controller if the I/O line never goes high.

36. Wait On I/O Low

0x89,

This will cause the controller to wait until GPIOH1 (MPSSE) or I/O1 (MCU Host Emulation) is low. Once the pin is detected as low, it will move on to process the next instruction. The only way out of this will be to disable the controller if the I/O line never goes low.

Document Revision History

AN2232C-01 Version 1.0 – Initial document created March 2004.

AN2232C-01 Version 1.1 – Initial document created April 2004.

- Signal names made consistent with FT2232C datasheet.
- Page 1 - Overview rewritten. FT2232C pin names added to data bit definition table.
- Pages 3, 4, 7 and 8 - Command names updated.
- Page 13 - Set TCK/SK Divisor expanded. Further examples added.

Disclaimer

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