Test Bit File
V1.0

INSTRUCTION (1 BYTE)	DATA	RETURNS
00 Port Alive Query	None	55 to signify port is up

INSTRUCTION (2 BYTES)	DATA	RETURNS
10 Return Specified Register	00 BOARD ID	NN = byte board ID
	01 FPGA ID	NN = byte FPGA ID
	02 DESIGN ID	NN = byte design ID
		E1 if data > 2 specified
20 Loopback next (data) byte	NN Loopback Value	NN = Loopback value
21 Loopback byte 2s comp	NN Loopback Value	MM = two's comp (NN)
30 Read Pin	NN pin number	Return state of pin NN
		E4 if NN = 1D, or >29
40 Assert Pin Low	NN pin number	Set output pin NN = 0
		E2 if NN = E, F, or >1E
41 Assert Pin High	NN pin number	Set output pin NN = 1
		E3 if NN = E, F, or >1E

INSTRUCTION (4 BYTES)	DATA	RETURNS
50 Read SRAM	NN Address Hi	YY = Data at address
	MM Address Mid	
	PP Address Lo	

INSTRUCTION (5 BYTES)	DATA	RETURNS
60 Write SRAM	NN Address Hi	ZZ = echo data written
	MM Address Mid	
	PP Address Lo	
	YY Data value	

Note: Board will return E0 if any command sent <> 10,20,21,30,40,41,50 or 60

Pin number definitions for Read Pin (0x30 NN)

NN (dec)	NN (hex)	Net Name	FPGA Pin	JP2 Pin
0	0	user_io(0)	U5 pin 58	JP2 pin 2
1	1	user_io(1)	U5 pin 59	JP2 pin 4
2	2	user_io(2)	U5 pin 93	JP2 pin 5
3	3	user_io(3)	U5 pin 94	JP2 pin 6
4	4	user_io(4)	U5 pin 96	JP2 pin 7
5	5	user_io(5)	U5 pin 97	JP2 pin 8
6	6	user_io(6)	U5 pin 103	JP2 pin 9
7	7	user_io(7)	U5 pin 104	JP2 pin 10
8	8	user_io(8)	U5 pin 105	JP2 pin 12
9	9	user_io(9)	U5 pin 106	JP2 pin 13
10	A	user_io(10)	U5 pin 112	JP2 pin 14
11	B	user_io(11)	U5 pin 113	JP2 pin 15
12	C	user_io(12)	U5 pin 116	JP2 pin 16
13	D	user_io(13)	U5 pin 117	JP2 pin 17
14	E	user_in(14) [INPUT ONLY!]	U5 pin 119	JP2 pin 18
15	F	user_in(15) [INPUT ONLY!]	U5 pin 120	JP2 pin 19
16	10	user_io(16)	U5 pin 122	JP2 pin 20
17	11	user_io(17)	U5 pin 123	JP2 pin 21
18	12	user_io(18)	U5 pin 124	JP2 pin 22
19	13	user_io(19)	U5 pin 125	JP2 pin 27
20	14	user_io(20)	U5 pin 126	JP2 pin 29
21	15	user_io(21)	U5 pin 130	JP2 pin 30
22	16	user_io(22)	U5 pin 131	JP2 pin 31
23	17	user_io(23)	U5 pin 132	JP2 pin 32
24	18	user_io(24)	U5 pin 134	JP2 pin 33
25	19	user_io(25)	U5 pin 135	JP2 pin 34
26	1A	user_io(26)	U5 pin 139	JP2 pin 35
27	1B	user_io(27)	U5 pin 140	JP2 pin 36
28	1C	user_io(28)	U5 pin 142	JP2 pin 37
30	1E	user_in(0)	U5 pin 10	JP2 pin 49
31	1F	user_in(1)	U5 pin 12	JP2 pin 48
32	20	user_in(2)	U5 pin 29	JP2 pin 47
33	21	user_in(3)	U5 pin 31	JP2 pin 46
34	22	user_in(4)	U5 pin 36	JP2 pin 45
35	23	user_in(5)	U5 pin 38	JP2 pin 44
36	24	user_in(6)	U5 pin 41	JP2 pin 43
37	25	user_in(7)	U5 pin 47	JP2 pin 42
38	26	user_in(8)	U5 pin 48	JP2 pin 41
39	27	user_in(9)	U5 pin 66	JP2 pin 39
40	28	user_in(10)	U5 pin 69	JP2 pin 38
29, >40	1D, >29	Returns read pin error E4	n/a	n/a

Pin number definitions for Write Pin (0x40/0x41 NN)

NN (dec)	NN (hex)	Net Name	FPGA Pin	JP2 Pin
0	0	user_io(0)	U5 pin 58	JP2 pin 2
1	1	user_io(1)	U5 pin 59	JP2 pin 4
2	2	user_io(2)	U5 pin 93	JP2 pin 5
3	3	user_io(3)	U5 pin 94	JP2 pin 6
4	4	user_io(4)	U5 pin 96	JP2 pin 7
5	5	user_io(5)	U5 pin 97	JP2 pin 8
6	6	user_io(6)	U5 pin 103	JP2 pin 9
7	7	user_io(7)	U5 pin 104	JP2 pin 10
8	8	user_io(8)	U5 pin 105	JP2 pin 12
9	9	user_io(9)	U5 pin 106	JP2 pin 13
10	A	user_io(10)	U5 pin 112	JP2 pin 14
11	B	user_io(11)	U5 pin 113	JP2 pin 15
12	C	user_io(12)	U5 pin 116	JP2 pin 16
13	D	user_io(13)	U5 pin 117	JP2 pin 17
14	n/a	user_io(14) [INPUT ONLY!]	U5 pin 119	JP2 pin 18
15	n/a	user_io(15) [INPUT ONLY!]	U5 pin 120	JP2 pin 19
16	10	user_io(16)	U5 pin 122	JP2 pin 20
17	11	user_io(17)	U5 pin 123	JP2 pin 21
18	12	user_io(18)	U5 pin 124	JP2 pin 22
19	13	user_io(19)	U5 pin 125	JP2 pin 27
20	14	user_io(20)	U5 pin 126	JP2 pin 29
21	15	user_io(21)	U5 pin 130	JP2 pin 30
22	16	user_io(22)	U5 pin 131	JP2 pin 31
23	17	user_io(23)	U5 pin 132	JP2 pin 32
24	18	user_io(24)	U5 pin 134	JP2 pin 33
25	19	user_io(25)	U5 pin 135	JP2 pin 34
26	1A	user_io(26)	U5 pin 139	JP2 pin 35
27	1B	user_io(27)	U5 pin 140	JP2 pin 36
28	1C	user_io(28)	U5 pin 142	JP2 pin 37
14, 15, >30	E, F, >1E	Returns write pin error of E2 for pin clear (low), or E3 for pin set (high)	n/a	n/a